Henan Wang

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RESEARCH INTERESTS

Device–circuit co-design and DTCO for emerging memory and spintronic devices, spanning device physics, compact modeling, digital/analog/mixed-signal circuits, and BEOL-compatible monolithic CMOS+X integration.

EDUCATION

Purdue University, West Lafayette, IN Aug 2023 – May 2027
Bachelor of Science in Electrical Engineering *Concentration:* Microelectronics and Semiconductors
GPA: 3.88/4.00

- **Relevant Coursework:** Semiconductor Memory Technologies, CMOS Analog Design, Digital Design, Nanoelectronics, Microprocessor Systems and Interfacing, Electromagnetics, Structure and Properties of Materials
- **Honors/Awards:** Purdue Summer Undergraduate Research Fellowship (SURF) with Distinction, 2026
  Dean's List and Semester Honors, six semesters

PUBLICATIONS AND MANUSCRIPTS

Under Review

[1] Z. Lin*, **Henan Wang***, et al., "Realizing Dual-Mode Memristor Based on $Ni_{0.8}Fe_{0.2}$-BTO/BTO/ $Ni_{0.8}Fe_{0.2}$-BTO Tri-layer Vertically Aligned Nanocomposites," *Small*, currently under major revision. *Co-first authors.

In Preparation

[2] **Henan Wang**, et al., "A CeO_2: Au Vertically Aligned Nanocomposite Memristor: From Nonideal Switching Dynamics to Model-Informed Conductance Multilevel Programming," manuscript completed; planned for submission to IEEE EDTM 2027.

Additional co-authored manuscripts in preparation: MTJ spin-dependent transport, MTJ-based p-bit circuits.

RESEARCH EXPERIENCE

Undergraduate Researcher Jan 2025 – Present
Purdue University, School of Electrical and Computer Engineering | Wang's Thin Film Group
Undergraduate Research Assistant, Summer 2025

Focus 1: RRAM Devices, Compact Modeling, and Device-Aware Programming and Neuromorphic Simulation

- Fabricate vertically aligned nanocomposite (VAN) RRAM via PLD and sputtering; correlate microstructure and interfaces with switching, multilevel and pulse-driven synaptic behavior using probe station, XRD, ellipsometry, AFM, and TEM; automate characterization and parameter extraction through MATLAB/Python workflows.
- Developed a measurement-calibrated behavioral compact model, achieving 0.042-decade MAE in 10-s settled state prediction; experimentally validated model-informed program-and-verify control, improving ± 0.05-decade targeting from 22% to 94% while cutting mean pulses from 3.3 to 2.7. [2]
- Built a device aware crossbar simulation for the dual mode memristor, extracting update nonlinearity, polarity reversal steps, C2C/D2D variation, read/write noise, and retention from raw pulse data; with write-verified differential-pair synapses, reached 92.7% MNIST accuracy (96.2% software) . [1]

Focus 2: Thin-Film Heterostructures and Device Physics

- Co-develop thin film material systems, growth conditions, and mechanism hypotheses for ferroelectric/ferromagnetic, VO_2 phase change, and 2D-barrier devices; investigate how heteroepitaxy, strain, interfaces, defects, and nanocomposite morphology govern ferroic, magnetic, optical, and electronic properties.
- Investigate transport and switching physics in multifunctional magnetic tunnel devices, including spin-dependent tunneling, nonvolatile-state retention, stochastic switching, and optical control of stochasticity; correlate material structure and device transport to identify mechanisms underlying deterministic and probabilistic operation.

Undergraduate Researcher Jun 2026 – Present
Purdue University, Birck Nanotechnology Center | NanoX Lab
Summer Undergraduate Research Fellowship (SURF) with Distinction, Summer 2026

Focus 1: BEOL Integration and Automated Characterization of CMOS+X (Emerging-Device) Systems

- Developing low temperature, BEOL-compatible CMOS+X integration workflows for depositing emerging device structures directly on post-CMOS coupons, with emphasis on MTJ and emerging-transistor technologies, including surface/interface preparation, process compatibility, and device-on-CMOS integration.
- Expanding hands on cleanroom fabrication capabilities through training and qualification in lithography, thin film deposition, and etching processes for CMOS+X device integration.
- Built an NI PXIe-based characterization platform integrating multi-channel SMUs, digital-pattern instruments, and FPGA resources for electrical validation of emerging devices and integrated CMOS+X prototypes.

Focus 2: MTJ p-Bit Reversible Full-Adder for Stochastic Computing (in production at TSMC)

- Contributed to RTL design, debugging, and mixed-signal integration of an MTJ p-bit based reversible full-adder for stochastic and probabilistic computing.
- Designed, simulated, and laid out MUX and inverter circuits for MTJ output selection and signal restoration; developed Verilog-A stochastic device models and RTL-compatible analog-macro interfaces.

Circuit & Hardware Design Projects

Senior Design – Programmable Bias-Voltage DAC Aug 2026 – Present

- Developing a programmable bias-voltage DAC in Cadence Virtuoso to tune the power–noise–speed trade-off of a collaborator-designed $\Sigma\Delta$ modulator.
- Built and simulated a 3-bit charge-redistribution DAC using a binary-weighted TSMC 65 nm MIM capacitor array and ideal switches; verified a 499.996 mV output against the 500 mV target for code `100`.
- Designed and simulated a standalone CMOS transmission gate in TSMC 65 nm; evaluated transistor sizing effects on settling and characterized an approximately 3.2 mV turn-off voltage step on a 111 fF capacitor load.

Fixed-Point Digital Attention Accelerator *Chips and AI Hackathon (Solo)* Jul 2026 – Present

- Designed a synthesizable signed-int8 scaled dot-product attention accelerator spanning MAC, dot-product, matrix multiplication, systolic-array, QK^T, LUT-based exponential, fixed-point normalization, and PV datapaths.
- Replaced 16 sequential probability divisions with four row-wise reciprocal operations and multiply-and-round normalization, reducing attention latency from 577 to 205 cycles (2.81×) while preserving bit-accurate fixed-point behavior across 216 RTL and post-layout GLS test cases.
- Integrated a 16×64-bit dual-port hard-memory macro and redesigned the memory-to-compute dataflow with dual-bank ping-pong buffering, eliminating a 48-cycle serial feed and reducing steady-state task interval from 329 to 213 cycles (1.54×); completed TSMC N40 RTL-to-GDSII closure with Tempus setup/hold slack of +0.046/+0.030 ns at 100 MHz.

Precision Bandgap Voltage Reference *AMS Team Member* Jun 2025 – Dec 2025

- Independently designed and simulated an approximately 1.5 V CMOS bandgap reference in Cadence Virtuoso/Spectre, combining PTAT and CTAT components and optimizing device/resistor ratios for first-order temperature compensation.
- Achieved 5.7 ppm/°C nominal TC over -40 to 125 °C, $<$ 1% Monte Carlo output variation, and 60 dB PSRR at 100 kHz.

SoCET – AFTx07 (Taped-Out): DFT *Test Engineering Team Member* Jan 2025 – May 2025

- Customized a Synopsys Fusion Compiler flow for UART block RTL synthesis, timing/area constraints, optimization, technology mapping, and gate-level netlist export.
- Inserted 4 scan chains with zero DFT DRC violations and developed stuck-at ATPG; the team generated 62 scan patterns and achieved 99.18% stuck-at test coverage on the UART block.

SELECTED PRESENTATIONS

Henan Wang, "Design of an Automated Characterization Infrastructure for CMOS+X Integrated Systems," *Purdue Undergraduate Research Conference: 2026 Summer Symposium*, West Lafayette, IN, Jul. 2026. **Poster presentation.**

Henan Wang, "Design and Characterization of a Precision Bandgap Voltage Reference for CMOS Analog Systems," *Purdue Undergraduate Research Conference: 2025 Fall Expo*, West Lafayette, IN, Nov. 2025. **Oral presentation.**

S. Hong, **Henan Wang**, et al., "SoCET-Test Engineering," *Purdue Undergraduate Research Conference: 2025 Spring Conference*, West Lafayette, IN, Apr. 2025. **Oral presentation; contributing team member.**

TEACHING EXPERIENCE

ECE 20001 – Electrical Engineering Fundamentals | Undergraduate Teaching Assistant 3 Semesters

- Held office hours and answered technical questions in person and on Piazza, supporting students in circuit analysis and introductory electrical engineering concepts.
- Proctored examinations and graded assignments, quizzes, and exams.

SKILLS

Device Fabrication: PLD, sputtering, photoresist spin coating, maskless direct-write photolithography (Heidelberg MLA150), wet/dry etching

Device Characterization & Test Automation: XRD, ellipsometry, AFM, TEM sample preparation, probe station, PMU/SMU, oscilloscope, NI PXIe, VISA-based instrumentation, modular DC/pulse measurement workflows, automated data logging and analysis

IC / Hardware Design: Cadence Virtuoso/Spectre, Cadence Genus/Innovus/Tempus, Synopsys Fusion Compiler/TestMAX, Verilog/SystemVerilog, Verilog-A, Altium Designer, EasyEDA

Programming & Data Analysis: Python, C/C++, MATLAB, Origin, SPICE, MNSIM